

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Geum-jong Bae et al.

Serial No.: 10/685,116

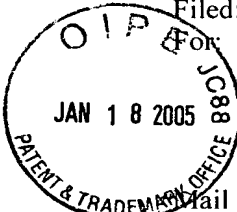
Filed: October 14, 2003

Group Art Unit: 2811

Examiner: Douglas W. Owens

Confirmation No.: 4438

For: CMOS INTEGRATED CIRCUIT DEVICES AND SUBSTRATES HAVING BURIED
SILICON GERMANIUM LAYERS THEREIN AND METHODS OF FORMING SAME



Date: January 14, 2005

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

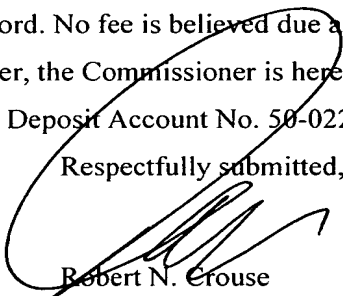
**RESUBMISSION OF INFORMATION DISCLOSURE STATEMENT
AND REFERENCES CITED ON THE PTO-1449**

Sir:

The attached list of documents on form PTO-1449 together with a copy of each identified document was previously submitted to the Patent Office on October 14, 2003 concurrent with the filing of the application. The copies of the foreign references provided on the PTO-1449 appear to have been illegible. Accordingly, Applicant provides herewith copies of each of the foreign references cited on the PTO-1449 as requested by Examiner Douglas W. Owens in an Office Action mailed September 17, 2004.

Applicant respectfully requests that the documents listed on the PTO-1449 be considered by the Examiner and officially made of record. No fee is believed due as this is merely a resubmission of previously submitted materials. However, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 50-0220.

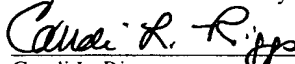
Respectfully submitted,


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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450 on January 14, 2005.


Candi L. Riggs

FORM PTO-1449 U.S. Department of Commerce Patent and Trademark Office				Attorney Docket Number 5649-839CT		Serial No. 10/685,116	
LIST OF DOCUMENTS CITED BY APPLICANT (Use several sheets if necessary)							
Applicants: Bae et al.							
Filing Date: October 14, 2003						Group 2811	
U. S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation Yes No
	1.	WO 97/23000	06/26/97	PCT	H01L29	78	
	2.	JP 9-321307	02/24/03	Japan	H01L29	786	No
	3.	JP 9-321307 Abstract	02/24/03	Japan	H01L29	786	Yes
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
	4.	Alieu et al., "Multiple SiGe well: a new channel architecture for improving both NMOS and PMOS performances," 2000 Symposium on VLSI Technology Digest of Technical Papers, pp. 130-131					
	5.	Mizuno et al., "High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," 1999 IEEE, IEDM, pp. 934-936					
	6.	"Sim et al., "Elimination of Parasitic Bipolar-Induced Breakdown Effects in Ultra-Thin SOI MOSFET's Using Narrow-Bandgap-Source (NBS) Structure," IEEE Transactions on Electron Devices, Vol., 42, No. 8, August 1995, pp. 1495-1502					
	7.	Yoshimi et al., "Suppression of the Floating-Body Effect in SOI MOSFET's by the Bandgap Engineering Method Using a Si _{1-x} Ge _x Source Structure," IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pp. 423-429					
	8.	Notice to Submit Response for Korean Patent Appln. 10-2000-0075482					
	9.	Search Report, GB 0100209.6, November 14, 2001					

 EXAMINER
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DATE CONSIDERED

Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.